




UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,386	08/26/2003	Noriyoshi Shimizu	300.1123	2050
21171	7590	08/05/2004	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			PAREKH, NITIN	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 08/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/647,386	Applicant(s) SHIMIZU ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) 7-9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. 09/044,444 filed on 09/04/03.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I, claims 1-6 in Paper No. 2 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US Pat. 6392898) in view of Koning et al. (US Pat. 6480370).
5. Regarding claims 1, 4 and 6, Asai et al. disclose a semiconductor package provided with a multilayer interconnect (MLI) structure (100 in Fig. 1) for mounting a semiconductor chip (not shown in Fig. 1; see 80 in Fig. 12) numerically referenced on its top surface, wherein:
 - a topmost stacked structure of the multilayer interconnect structure includes a capacitor structure (metallization-158U/insulating resin 146/metallization 58U in Fig. 1-9), said capacitor structure having a dielectric/insulating layer comprised of

a mixed layer of an inorganic filler and insulating resin (146 in Fig. 1-9; Col. 7, line 65- Col. 8, line 8; Col. 7-9),

- the MLI comprising a plurality/stack of the capacitor structures including those on the top and bottom surfaces of the package (see the MLI structure in Fig. 1), and
- the structure including the chip electrodes being directly connected to the chip connection pads (see 76U and 160U in Fig. 1 and 12) and further being directly connected with the top electrodes and bottom electrodes (75U and 58U/60U respectively in Fig. 1-9)

(Fig. 1-9; Fig. 12; Col. 5, line 60- Col. 12, line 25; Col. 1-12).

Asai et al. fail to teach the dielectric layer comprising a high dielectric constant filler.

Koning et al. teach using a conventional ceramic dielectric layer having a high dielectric constant filler/powder of ceramic such as barium or lead titanate having a perovskite structure to provide a high dielectric constant and the desired electrical properties for the insulating dielectric layer (Col. 5, line 2; Col. 2, line 5)

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the dielectric layer comprising a high dielectric constant filler as taught by Koning et al. so that the desired electrical properties can be achieved and the device performance can be improved in Asai et al's package.

Regarding claims 1 and 2, forming the dielectric layer do not distinguish over Asai et al. and Koning et al., because only the final product/structure is relevant, not the process of forming the dielectric layer such as “electrodepositing”, “electroless plating”, “spraying” or using “chemical vapor deposition (CVD)”. Note that a “product by process” claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claims 2 and 3, Asai et al. and Koning et al. teach substantially the entire structure as applied to claim 1 above, wherein Asai et al. further teach:

- the MLI structure being on top and bottom surfaces of an insulating substrate (see 30 in Fig. 1; Col. 8, line 38), and

- the chip electrodes being inside a region superposed with said capacitor structure in a plan view (see 76U and the capacitor structure under the chip 80 in Fig. 12).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US Pat. 6392898) and Koning et al (US Pat. 6480370) as applied to claim 1 above, and further in view of Lauffer et al. (US Pat. 5796587).

Regarding claim 5, Asai et al. and Koning et al. teach substantially the entire structure as applied to claim 1 above, except the insulating resin being a polyimide resin.

Lauffer et al. teach using a dielectric resin comprising conventional resin such as a polyimide resin (Col. 3, line 46).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the polyimide resin as taught by Lauffer et al. so that the desired electrical properties can be achieved and the device processing can be simplified in Asai et al's package.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

Art Unit: 2811

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

08-02-04



NITIN PAREKH

PATENT EXAMINER

TECHNOLOGY CENTER 2800